Brief Papers

Impact of Clock Slope on True Single Phase Clocked (TSPC) CMOS Circuits

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Abstract—**Clocked digital circuits are sensitive to changes of the input signals close to the clock transitions. Non ideal properties of the clock transition, such as slope, make timing requirements more complicated. Here we present methods, quantitative limits and clock buffer requirements by studying clock slope impact on TSPC [1] circuits. The investigation is based on SPICE simulations of edge-triggered D flip-flops and latches, implemented in the TSPC technique. The simulation results were also verified by measurements on 2-μm CMOS prescalers.**

I. Introduction

THE outputs of most digital circuits do not depend on the rise or fall times of the input signals. However, large rise and fall times on the clock signal might generate errors as we will discuss here. During the clock transitions, both NMOS and PMOS transistors conduct simultaneously, which might cause latches and delay elements to be transparent. This can be avoided by using several nonoverlapping clock signals, but if we choose a simpler clock signal generation and distribution the clock slope requirements need to be fulfilled. To avoid a large waste of area and power dissipation we have to know the requirements and design an appropriate clock buffer. To find the slope requirements we need to understand why the circuits fail when the rise and fall times increase.

With the results presented here, we propose how to find clock slope requirements and how to design the clock buffer. We also suggest how to test circuits with clock slope related problems. Methods and results are based on simulations and measurements of TSPC circuits, but methods and general results are believed to be valid also for other clocking strategies that do not use nonoverlapping clock phases.

II. Definitions Regarding Slope and Time

When studying timing related issues a window technique using setup time and hold time is often used. The setup time for signal A with respect to signal B is defined as the required time for signal A to be stable before a transition occurs for signal B. The hold time is defined as the period after the transition of signal B where signal A is not allowed to change. For the sake of generality, both the setup and hold time can be less than zero but the sum of them can never be negative and there will always be a "forbidden" window where the input signals have to be stable. For most circuits the ordering of two input signals is only important when one of the signals is the clock. Therefore, the setup and hold time of an input signal is often given with respect to the clock signal.

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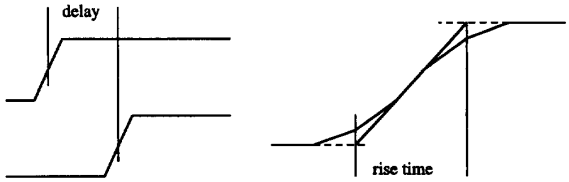

Fig. 1. When comparing two signals the 50% levels are used and when describing the slope of a signal, the time derivative at 50% level is used.

When dealing with signals that have finite slope we need a definition of both when a transition occurs and how large the slope is. When comparing the time difference between two signals the 50% levels will be used as shown in Fig. 1. Describing the slope of a signal, the transition of the signal is linearized, using the time derivative at $V_{dd}/2$ as coefficient, i.e., slp $= dV/dt$ at $V = V_{dd}/2$. The rise time is then defined as $V_{dd}/(dV/dt)$.

From these definitions, the circuit to be studied concerning setup and hold times needs at least one output and two input signals. The smallest unit to be studied could be a single transistor used as a transmission gate. For the D flip-flop in Fig. 2 the smallest part with two inputs and one output is a clocked inverting stage. It is necessary to divide the flip-flop into three such stages, else internal slope related problems cannot be discovered.

III. SPICE Simulations

Since the propagation delays of CMOS circuits depend on the input slope [3], we can expect the setup and hold times to depend on the clock slope. Finite slope causes NMOS and PMOS transistors to conduct simultaneously. Therefore, two stages that are supposed to work during different nonoverlapping clock phases might be transparent. The longer time the input signal is within the range V_{tn} to $V_{dd} + V_{tp}$ where both N and P transistors conduct, the larger is the risk of transparency. From this, we draw the conclusions that the effect of clock slope depend on V_{dd}, V_t, parasitic capacitances and transistor conductances.

The studied D flip-flop in Fig. 2 consists of three clocked inverting stages, which each have setup and hold times defined. The setup and hold times for all three stages were determined

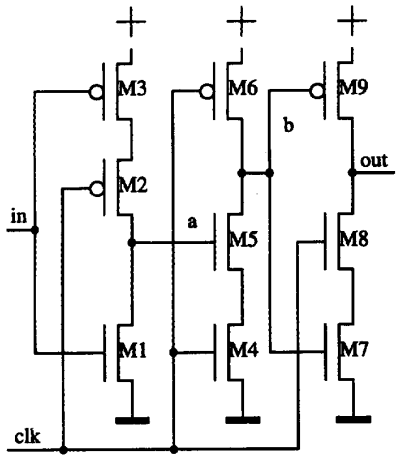

Fig. 2. True single phase clocked inverting positive edge triggered D flip-flop.

by SPICE simulations for different V_{dd}, input clock slope and process parameters. The setup and hold times for all three stages had a similar dependency and the results for the first stage will be presented. Three sets of SPICE parameters were used representing process variations, labelled as wp (worst power), tp (typical) and ws (worst speed). In the case of ws, the mobility and the channel narrowing is small while the parasitic capacitances and the threshold voltages are large. The wp parameters on the other hand, represent large mobility and channel narrowing but small capacitances and threshold voltages. The following results were obtained using transistors with $W/L = 10\ \mu m/2\ \mu m$.

The setup and hold times for the first stage are shown in Fig. 3 as a function of the process parameter set and the clock rise time. When clocking a very fast circuit with small propagation delay between two clocked stages, sharp clock transitions are required to have low hold times avoiding hold time violations. The hold time is lower for ws parameters, indicating that robustness against clock slopes can be achieved by using slower circuits. When designing a circuit we usually underestimate the speed of the circuit in simulations to guarantee the ability to run at a certain clock frequency despite process variations. Since the sensitivity to clock slope is larger for wp parameters we need to overestimate the speed when simulating the circuit to find worst case (sharpest) clock slope requirements. To find clock slope requirements in other processes, simulations of prescalers and shift registers are highly recommended since these circuits are likely to be the fastest, giving the toughest clock slope requirement.

The setup and hold times for the input stage as functions of V_{dd} and the clock slope are shown in Fig. 4. As expected the setup time decreases with increased voltage and the circuit can be clocked at a higher frequency. If we want a very robust circuit still having negative hold times for large rise times, the power supply can be reduced. The reason for increased robustness with decreased voltage is that finite slope only has effect when the clock signal is within the range

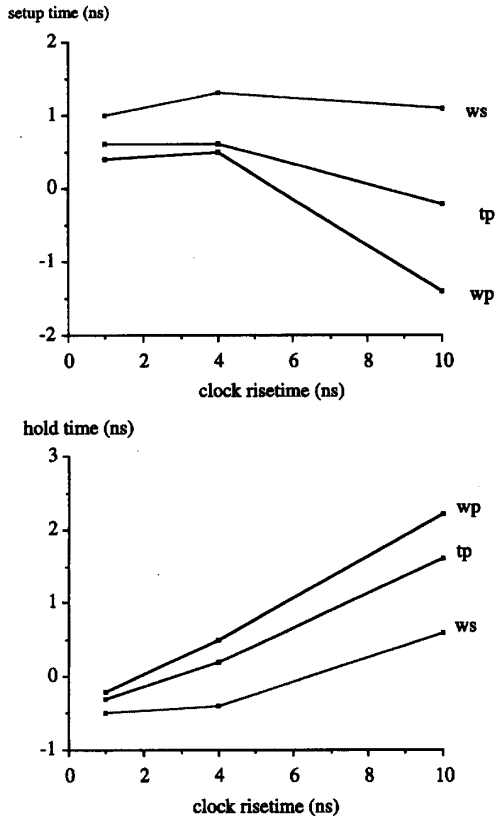

Fig. 3. Setup and hold times for one type of transition as functions of both the clock rise time and the process parameters.

V_{tn} to $V_{dd} + V_{tp}$. The ideal case would be to have $V_{dd} = V_{tn} - V_{tp} = 2 \cdot V_t$ where the slope ideally will have no effect. This observation makes it possible to test fabricated circuits even if there are clock slope failures. If the circuit does not work with standard power supply due to an insufficient clock buffer (giving large clock rise and fall times), the circuit will work when reducing V_{dd}.

IV. Circuit Measurements

Two different prescalers fabricated in a 2 μm CMOS process were available for measurements. The circuits consisted of a chain of dividers where each divider was realized by the inverting D flip-flop in Fig. 2 with a feedback from the output to the input and the output working as the clock signal to the following D flip-flop. The first divider of the chain was driven by an unbuffered input allowing change of the clock rise and fall times. The first divider of one of the chains was speed optimized using transistor sizing [2] while the first divider in the other chain had all widths set to 10 μm.

The four possible transitions for the divider are shown in Fig. 5 with node names according to Fig. 2. For case d1, the clock is rising which causes node b to fall and the output to rise. As the output is fed to the input, M1 will turn on, node a will fall and shut off M5. If the clock rise time is larger

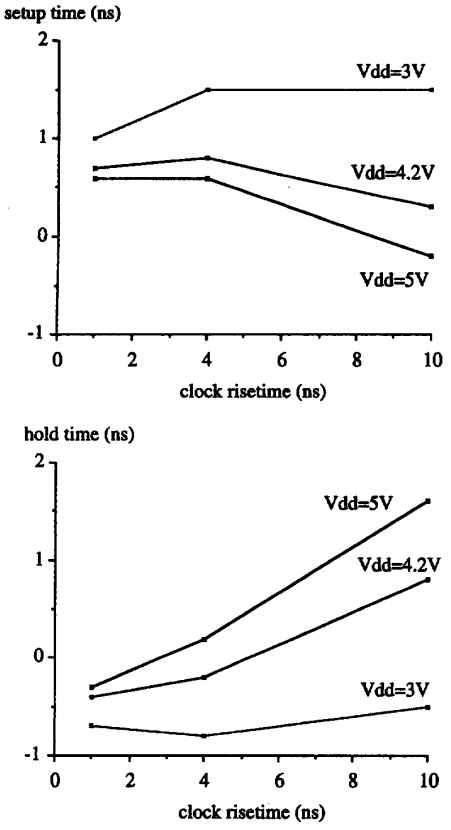

Fig. 4. Setup and hold times for one type of transition as functions of both the clock rise time and the power supply, V_{dd}.

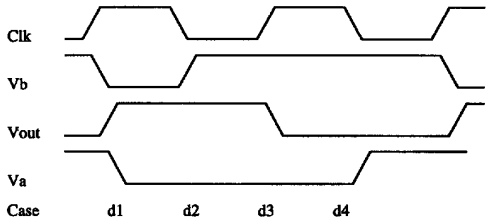

Fig. 5. Transitions and their dependency for input, output and the internal states of the divider.

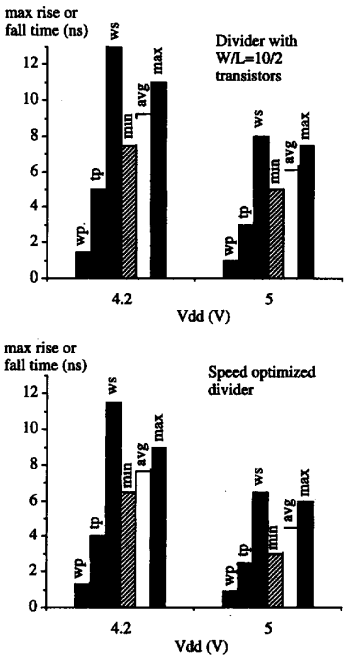

Fig. 6. Simulated and measured maximum allowed clock rise or fall times for a divider with $W/L = 10\ \mu$m/2 μm transistors and for a speed optimized divider.

than the propagation delay of this feedback, M5 is cut off before node b reaches a clear low state. Here the falling of node a violates the hold time of the middle stage. In case d2 the clock is falling and node b is precharged high. If node b rises too fast, the hold time requirement for the last stage will be violated and the output will fall since the clock has not cut off M8 fully due to clock slope. When the clock is rising in case d3, the output will fall and this low value is fed back to the input. If the clock has not yet cut off M2 there will be a hold time violation of the first stage, which causes node a to be erroneously charged. In the last case, the clock is falling causing node a to rise. If M4 is not cut off before a is high, there will be a dip on node b that propagates a high value to the output. In general we can say that when one inverting stage is triggered by the clock, the output of this stage will propagate to another clocked inverting stage and might violate its hold time restriction if the clock rise or fall time is too large compared to the propagation delay between these two stages.

In Fig. 6 the results from both SPICE simulations and measurements are given for both circuits when using $V_{\rm dd} = 5$ V and $V_{\rm dd} = 4.2$ V. The three leftmost bars represent the maximum allowed rise and fall times when using wp, tp and ws parameters in SPICE simulations. The three rightmost bars represent the maximum allowed rise and fall times from ten different chips with min, average and max values given within the sample. In the measurements, the circuit was considered to be working as long as it divided the input frequency by two while in the SPICE simulation an error was defined as one signal being 1 V deviated from its expected value for at least half a clock cycle. Therefore it should not be of great surprise that the required clock rise and fall times obtained from the simulations are slightly stricter than the measured ones. Again we can see that lower $V_{\rm dd}$ allows larger rise and fall times and faster circuits need sharper clock transitions for correct functionality. At a 3 V power supply it was possible to use rise and fall times of 100 ns. The maximum toggle frequency at $V_{\rm dd} = 5$ V for the unscaled divider was earlier reported to be 500–550 MHz and 650–750 MHz for the speed optimized version [2]. Therefore, there is no risk of slope failure when clocking the circuits at their highest possible frequency since a triangular wave at 500 MHz have a rise time less than 1 ns and at 700 MHz the rise time is less than 0.7 ns. The

requirements according to Fig. 6 are about a factor of 5 from these figures.

To get some process independent reference we also simulated an inverter chain. One inverter delay in a minimum size inverter chain was simulated to be 0.28 ns, 0.14 ns and 0.06 ns for ws, tp and wp parameters, respectively. The rise and fall time limit is then estimated to 20 minimum size inverter delays. We translated the clock buffer requirement as the maximum allowed fan out of the clock signal. To satisfy the slope requirements according to Fig. 6, the fan out of the clock buffer has to be less than 10–15 depending on process parameters. Clock distribution RC delays were not included in these simulations and to include a safety margin we can specify the maximum clock buffer fanout as 3–4, which is normal for microprocessors [4]. Simulations of a negative edge-triggered prescaler, precharged and non precharged TSPC latches [1] connected as shift registers show the same requirements. This shows that the results presented here are sufficient to describe the slope requirement of the TSPC technique.

V. Conclusion

The results presented show that slope dependent functionality failures due to non ideal clock transitions with finite slopes can be seen as a mismatch between the clock signal and the circuit. A fast circuit needs sharper transitions to work properly. Our results indicate that the clock rise and fall time limits are about two periods of the maximum clock frequency of the fastest subcircuit in a TSPC system. This is equivalent to 20 minimum size inverter delays and can be obtained with some safety margin by limiting the clock buffer fanout to 3–4.

Traditionally, setup and hold times have been defined for building blocks as D flip-flops and latches. We show that it is necessary to consider the setup and hold times for clocked inverting stages to discover internal timing problems in the building blocks. We explained clock slope failures by concidering setup and hold times of inverting stages as functions of the clock slope.

When testing fabricated circuits, clock slope related problems can be avoided using lower V_{dd}. From measurements of prescalers, the maximum allowed clock rise and fall times were 5–8 ns when having $V_{dd} = 5$ V. At $V_{dd} = 4.2$ V this figure increased by 50% and at $V_{dd} = 3$ V the circuits worked with an input rise time of more than 100 ns.

References

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[4] Comment by reviewer.