Noise in Digital Dynamic CMOS Circuits

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Abstract— **Dynamic logic is an attractive circuit technique giving reduced area and increased speed for CMOS circuits. Static logic has a major advantage: its superior noise margins. To be able to choose between a static and a dynamic implementation of a design, we need to know the requirements for dynamic logic. Here we try to identify possible errors, estimate the limits and discuss some possible solutions when considering noise in dynamic circuits.**

I. Introduction

FOR a given digital system there are several CMOS implementations for which speed, power consumption, simplicity and area differ. One of the first choices when going to implement a CMOS system is whether to use static or dynamic logic. A typical characteristic of precharged dynamic logic is lower transistor count with a reduced capacitive load that gives higher speed capability and reduced area [1]. Non-precharged dynamic logic does not have reduced transistor count when implementing logic evaluating functions, but latches and delay elements are simpler to build. Dynamic logic (especially precharged) seems to have many advantages compared with static logic, except for one issue, which is noise. In the following we will estimate noise limits and requirements for dynamic logic circuits.

There are three main differences between static and dynamic logic considering noise:

- Static logic may recover from noise induced logic errors if there is no loop in a circuit. Notice however that a static D flip-flop has a feedback loop that cannot recover from noise induced errors. Precharged dynamic logic cannot recover if the precharged node has been discharged by a noise pulse.
- Static logic contains both N and P structures that can be balanced to obtain highest possible noise margin. This is not the case for dynamic logic, which might have a noise margin as low as V_t.
- Highly synchronous logic will generate large current pulses by precharging and evaluating many nodes simultaneously causing dI/dt noise. If many nodes are precharged in dynamic logic, the noise levels might be higher than for static logic.

In this paper we will discuss noise sensitivity and noise generation of dynamic circuits. Theory, simulations and measurements will be covered.

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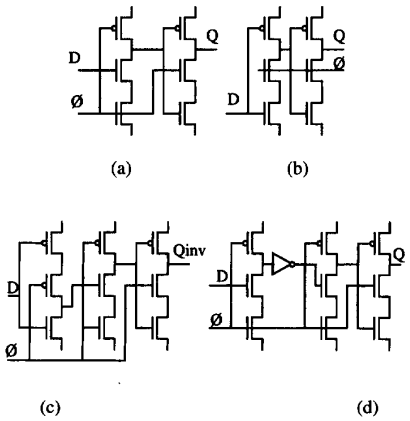


Fig. 1. N type TSPC blocks. (a) Precharged N latch, (b) non precharged N latch, (c) positive edge triggered D flip-flop, (d) N type domino block.

II. TSPC Dynamic Logic and CMOS Process Parameters

When discussing noise sensitivity and noise generation we will give some circuit examples using a circuit technique called TSPC (True Single Phase Clock) [3] that distributes only a single clock wire throughout a complete chip. All noise analysis methods presented are similar, however, to other dynamic clocking techniques, so we expect our methods to be easily extended to other clocking strategies. Fig. 1(a) illustrates a precharged dynamic N type latch that evaluates at high clock phase while the output is latched at low clock. A non precharged version of the N latch is shown in (b). Fig. 1(c) illustrates a precharged inverting positive edge triggered D flip-flop while an D type domino circuit is shown in (d). Any transistor that is not clocked can be replaced by a logic evaluating network of transistors making logic placement very flexible. Four complementary P blocks are also available and should be alternated with N blocks when building circuits [3].

In all circuit examples given below we use a standard 1 μm CMOS bulk process available to us, shown in Table I.

III. Possible Noise Errors and Noise Sensitivity

A general MOS circuit has input signals, internal dynamic nodes and Vdd and Gnd terminals on which harmful noise pulses might appear. A circuit also has internal static nodes on which noise pulses cannot change the logical state. Here we assume that static nodes have a low impedance path to either Vdd or Gnd that will eliminate noise on these nodes generated by sources other than Vdd and Gnd. To detect

TABLE I
DATA FOR A 1 μm CMOS PROCESS

Power supply	Vdd= 5 V	Threshold voltage	$V_t = 0.77$ V
Min. transistor length	$L_{\min} = 1\mu$m	Min. transistor width	$W_{\min} = 2.4\mu$m
Gate oxide thickness	$t_{ox} = 22$ nm	Field oxide thickness	$F_{ox} = 0.62$ nm
Electron mobility	$\mu_n = 540$ cm^2/Vs	Hole mobility	$\mu_p = 170$ cm^2/Vs
Metal1 min. width	$W_{M1} = 2\mu$m	Metal1 min. spacing	$d_{M1} = 1.4\mu$m
Metal1 thickness	$t_{M1} = 0.6\mu$m		
Poly min. width	$W_p = 1.0\mu$m	Poly min. spacing	$d_p = 1.2\mu$m
Poly thickness	$t_p = 0.35\mu$m		
Metal2 min. width	$W_{M2} = 2.4\mu$m	Metal2 min. spacing	$d_{M2} = 1.6\mu$m
Metal2 thickness	$t_{M2} = 1.0\mu$m		

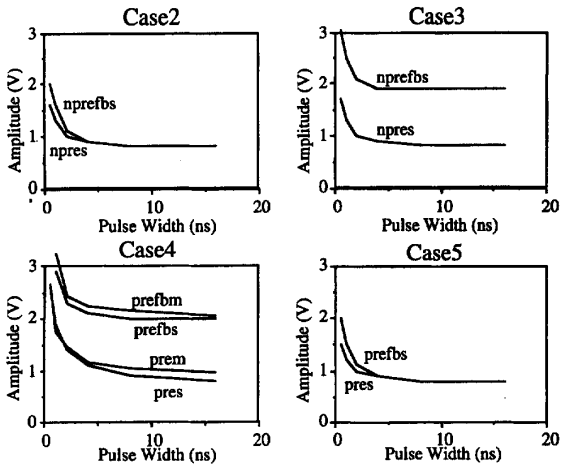


Fig. 2. Noise immunity curves show maximum allowed noise pulse amplitude for a certain pulse width. A larger amplitude will generate an error while a smaller amplitude is harmless. Characters in the abbreviations denote the following: npre = nonprecharged N latch, pre= precharged N latch, fb = weak feedback according to Fig. 4(a), s = simulated results, m = measured results.

possible logical errors in dynamic circuits, we first identify possible dynamic nodes in the circuit to be studied. Then we find out what signal combination is required to bring the circuit into the state that produces these dynamic nodes and what kind of noise pulse might cause any dynamic node to change state. For the N latches in Fig. 1(a) and (b), we have detected the following cases. Cases 1–3 below might occur in a non precharged latch while cases 4–5 describe dangerous situations for a precharged latch.

Case 1: If the input of a nonprecharged N latch (Fig. 1(b)) has been rising after the falling edge of the clock, the middle node is dynamic high and the output is dynamic low. A negative glitch on the middle node (or a positive glitch on Vdd) may cause the output to rise.

Case 2: The output of a nonprecharged N latch will be dynamic high at low clock if the input has been falling after the falling clock edge. A positive glitch on the clock signal (or a negative glitch on ground) may cause the output to fall.

Case 3: Another type of error might occur for the signal combination in case 1. A positive glitch on the clock (or a negative glitch on ground) may cause the middle node to fall and the output to rise.

Case 4: If there is a positive glitch on a low input (or a negative glitch on ground) while the clock is high on a precharged N latch (Fig. 1(a)), the precharged node might fall.

Case 5: The same situation as in case 2 is valid for precharged latches.

Both amplitude and duration of a noise glitch are parameters that determine if there will be a logical error or not. A convenient way to specify the noise immunity in terms of both the amplitude and the duration of a noise pulse is described in [2]. Plotting the maximum allowed noise amplitude as a function of the noise pulse width in a diagram, the A-W (amplitude-width) plane will be divided into a safe and an unsafe region, as in Fig. 2. If the noise pulse is specified with a point in the A-W plane below the curve it will not affect the logical levels. Fig. 2 shows simulated noise immunity curves for precharged and nonprecharged N latches for case 2–5 above. The noise sensitivity of a precharged N latch in Fig. 1(a) was also measured on a chip. A short positive pulse was applied to a low input when the latch was evaluating as described in case 4 above. Table I gives the parameters for the CMOS process we used.

For large pulse widths the noise margin is about V_t, but weak feedback, introduced in the next section, increases the critical amplitude to about 2 V for cases 3 and 4. Weak feedback also improves the immunity against noise with short pulse width, but this is mainly due to increased capacitance of the dynamic nodes. Case 1 noise has the same characteristic as case 3 and is therefore omitted.

As a comparison with static logic we simulated a nand and a nor gate with three inputs each. The noise margins (NM), defined in [6], are plotted in Fig. 3. We also plot the switch point (SP) of the gates, where we define the switch point as the lowest input that can bring the output to Vdd/2. Both noise margin and switch point are plotted as functions of W_p/W_n, where W_p and W_n are the width of the P and N transistors, respectively. Worthwhile noting here is that a three input nor gate with unit size transistors has a worst case noise margin of about V_t, while the switch point is somewhat higher. These curves show only the noise margin for large pulse widths but for shorter pulses the noise immunity will be larger [10], in the same way as for the noise margin of dynamic circuits discussed above.

IV. ENHANCED NOISE IMMUNITY

To make circuits more robust against noise, non precharged latches were provided with a weak feedback in [5] shown in Fig. 4(a). This feedback transistor was sized so that it will supply enough current to cancel the effect

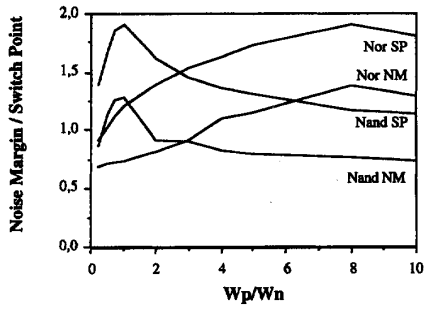


Fig. 3. Noise margin (NM) and switch point (SP) for 3-input nand and nor gates.

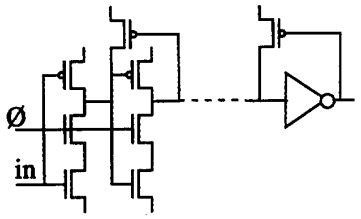


Fig. 4. (a) Weak feedback in last stage of an N latch increases noise immunity for cases 1, 3, and 4. (b) An external inverter with feedback increases noise immunity for case 2 and 5.

of noise. The noise immunity for cases 1 and 3 above can be increased by the feedback in Fig. 4(a), as shown in Fig. 2. However, this type of feedback does not improve the immunity against noise of types 2 and 5. An external inverter with feedback shown in Fig. 4(b) enhances the noise immunity for cases 2 and 5. The noise in case 4 can be cancelled by a weak feedback in the last stage shown in Fig. 4(a). Thus, the technique with weak feedback can provide enhanced noise margins for all types of noise.

Disadvantages with weak feedback are ratioed design, reduced speed and increased power consumption. The design becomes ratioed as the circuit function will depend on the size of the feedback transistor. Our results (Fig. 2) was obtained by using a feedback P transistor sized so that its strength is 1/5 of that of the two serial N transistors in the first stage of the latch (Fig. 4(a)). For the N latch case this is not a problem, but for a P latch we need a very long feedback N transistor (as its inherent strength is higher than that of P transistors), which gives rise to a large capacitance. An alternative to weak feedback would be to exploit the increased noise margin for short noise pulse widths. If all noise pulses are shorter than 1 ns and have an amplitude less than 1 V the noise would cause no logical errors as indicated by the plots in Fig. 2. This conclusion is not entirely true as explained in the following. If a 1 V positive glitch appears in the ground wire, this glitch will propagate to the output of a P latch while the clock is low. At a rising clock edge, the output of a P latch might be latched at the peak value of the glitch. Therefore, the following circuit will receive a noise pulse with a width equivalent to half a clock period. To prevent logical errors it is necessary that the following circuit has a high "DC" noise margin, i.e., a static gate (inverter or nand) or a latch with weak feedback. This reminds us of a "folklore" rule saying: A dynamic node is not allowed to drive another dynamic node [15]. As a summary we suggest the following for dynamic logic:

- If the noise levels are less than V_t, no noise immunity enhancement is necessary.
- If the noise levels are slightly higher than V_t, a dynamic node is not allowed to drive another dynamic node. To eliminate such structures, insert a static gate between the dynamic nodes or make one of them appear static by utilizing weak feedback.
- If dynamic nodes store their values for a relatively long time (several clock periods), several short pulses are equivalent to a long pulse. Therefore the "DC" noise margin is valid, no matter the pulse width. Consequently, we need to make sure that the noise levels are less than the "DC" noise margin.
- If the noise levels are significantly higher than V_t, noise reduction is necessary by e.g., on-chip decoupling capacitance discussed later.

V. Noise Sources and Calculation of dI/dt Noise

There are many physical sources of noise as for example:

- many circuits evaluating simultaneously causing power supply fluctuations,
- capacitively coupled crosstalk from neighbouring wires [9],
- many off chip drivers switching simultaneously generating dI/dt noise [2],
- alpha particles generating charge in a dynamic node,
- electromagnetic radiation from external sources,
- external noise on the power supply of a chip.

We will not compare the relative importance of these noise sources. Instead we will use the first two sources as examples and estimate the noise levels generated by these.

When several circuits suddenly evaluate, there will be a current pulse in the power supply network. This will cause a voltage pulse on the ground level equivalent to $\Delta V = L_{\text{gnd}} \cdot dI_{\text{gnd}}/dt + R_{\text{gnd}} \cdot I_{\text{gnd}}$, where L_{gnd} is the inductance and R_{gnd} is the resistance in the ground path. Assuming that the resistance can be kept low [8], we will model the inductive part of the noise generated by TSPC logic presented above. The P latch in Fig. 5(a) will precharge the middle node at rising clock edge as in Fig. 5(c). In addition to the precharge current of P latches, N latches will generate an evaluation current at rising clock edge. The current flowing from the middle node in Fig. 5(b) can be written:

$$i_m(t) = (C_p + C_n) \cdot \frac{dV_m}{dt}. \tag{1}$$

Here we have neglected the inductance, assuming the power supply fluctuation to be small. The current coming from the anode of C_n will go to the cathode while the current flowing from C_p will continue through the ground wire. Thus, the current in the ground wire (i_{gnd}) can be written:

$$i_{\text{gnd}}(t) = C_p \cdot \frac{dV_m}{dt} = \frac{C_p}{C_p + C_n} \cdot i_m(t). \tag{2}$$

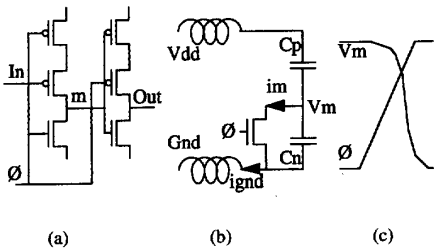


Fig. 5. (a) Precharged TSPC P latch. (b) Simplified model when studying noise generation of a P latch. (c) The middle node of the latch in (a) is precharged low at rising clock.

Assuming the inductance of the power supply path, L_{gnd}, is the main cause of noise, the noise on the ground wire will approximately be

$$V_{\text{gnd}}(t) = B \cdot L_{\text{gnd}} \cdot \frac{di_{\text{gnd}}}{dt} = B \cdot L_{\text{gnd}} \cdot C_p \cdot \frac{d^2V_m}{dt^2}, \quad (3)$$

where, B is the number of latches supported by current through the ground path. If standard domino logic (Fig. 1(d)) is used, B represents the total number of precharged nodes. V_{gnd} has its maximum where the V_m curve in Fig. 5(c) has a sharp convex shape. This occurs when the precharging N transistor is saturated so the current from the middle node can be written:

$$\begin{aligned} i_m(t) &= \frac{\beta n}{2} \cdot (\emptyset - V_t - V_{\text{gnd}})^2 \\ &= \frac{\beta n}{2} \cdot \left(\frac{t}{t_{\text{rclk}}} \text{Vdd} - V_t - V_{\text{gnd}}^2 \right) \end{aligned} \quad (4)$$

where, t_{rclk} is the rise time of the clock signal and $\emptyset = t/t_{\text{rclk}} \cdot \text{Vdd}$ for $0 < t < t_{\text{rclk}}$, is a linear approximation of the clock edge. (4) combined with (2) and (3) gives

$$\begin{aligned} V_{\text{gnd}}(t) = \frac{BL_{\text{gnd}}C_p\beta_n}{C_p + C_n} &\left(\frac{t}{t_{\text{rclk}}} \text{Vdd} - V_t - V_{\text{gnd}} \right) \\ &\cdot \left(\frac{\text{Vdd}}{t_{\text{rclk}}} - \frac{dV_{\text{gnd}}}{dt} \right). \end{aligned} \quad (5)$$

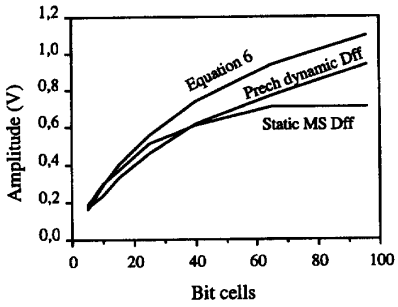
If we assume that the Vdd path has the same inductance as the Gnd path, Vdd will actually decrease by the same amount as the Gnd level is increasing. The maximum Gnd level, which we call x, is obtained when the time derivative of V_{gnd} is 0. Therefore, we rewrite (5) as

$$x = \frac{\text{BLC}_p\beta_n}{(C_p + C_n) \cdot t_{\text{rclk}}} \left\{ \frac{t}{t_{\text{rclk}}} (\text{Vdd} - x) - V_t - x \right\} \cdot (\text{Vdd} - x), \quad (6)$$

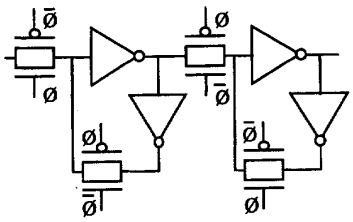
where, $t < t_{\text{rclk}}$. This shows that the strength of the precharging transistor and the clock rise time are important parameters determining the noise level.

For TSPC logic there is a requirement on the clock rise time to be less than about two clock periods of the maximum clock frequency of the fastest circuit, e.g., a shift register, in the system [4]. The simulated maximum clock rise time for precharged latches without weak feedback is 2 ns for our process. Some safety margin is desirable and therefore we specify the clock rise time as 0.75 ns.

In Section VII a precharged shift register is discussed. In Fig. 6(a) we compare the solution of (6) with the maximum



(a)



(b)

Fig. 6. (a) Maximum noise levels in the ground wire having 10 nH inductance. (b) Static master-slave flip-flop.

noise levels obtained in spice simulations of this shift register using the process described in Table I. We set t/t_{rclk} to 0.8 and reduce ß to 85% of its original value of 200 μA/V^2 due to short channel effects discovered in the simulations. As seen in Fig. 6, (6) predicts a more pessimistic value than obtained in spice simulations. The noise generation of the static master-slave flip-flop in Fig. 6(b) was also simulated for comparisons. The results show that the noise level is more dependent on the number of bit cells than whether a static or dynamic flip-flop is used.

A statistical approach will predict a lower noise level as explained in the following. The probability for the middle node of a P latch being charged high before precharging is 1/2 and the probability for an N latch evaluating its middle node low is also 1/2. Therefore, the x axis scale in Fig. 6(a) would be multiplied by a factor of two. If we assume that the main part of the power supply inductance is the bonding wire, we can calculate the maximum number of latches driven by a single bonding wire as a function of the maximum allowed noise level. If the maximum allowed noise amplitude is specified as Vdd/10, the maximum number of latches in our 1 μm process supplied by a single bonding wire with 10 nH inductance is about 50, if the factor 1/2 is considered.

VI. Crosstalk

The five cases of noise listed in Section III are not only caused by noise in the power distribution network, but also noise induced in dynamic nodes. This noise can be generated by, e.g., capacitive crosstalk, alpha particles

or electromagnetic radiation. In the following we will discuss limitations due to capacitive crosstalk to dynamic nodes. The main idea of this discussion is to develop a few process-dependent layout design rules from the theory presented in [9]. Capacitive crosstalk can be divided into two classes, crosstalk from neighboring/crossing wires and crosstalk through the gate-to-channel capacitance of a transistor. The latter will not be discussed here but was briefly mentioned in [5], [11].

The capacitance between two neighboring wires will cause a logic event on one wire to induce noise into the other wire. The physical geometry and an electrical equivalent of two neighboring wires are drawn in Fig. 7(a). If we consider the metal1 layer, the notation can be translated to our process as: $h = 2 \cdot F_{ox}, W = W_{M1}, t = t_{M1}$ and $d = d_{M1} + W_{M1}$. In [9] there is a coupling coefficient defined as $k_v = C_m/C_s$, where, C_m is the mutual capacitance between the wires per unit length and C_s is the total capacitance of each wire per unit length. For the process in Table I, the coupling coefficients are 0.12, 0.18 and 0.23 for poly, metal1 and metal2, respectively. These coupling coefficients put some restrictions on the layout of dynamically driven wires. Assume a dynamic node consists of a wire of length L, which has a neighboring wire of length x. We can further assume that each dynamically driven wire at least has two drains and two transistor gates as capacitive load. Specifying the maximum noise level on the dynamic node as $V_{dd}/10$ and estimating a drain capacitance to be equivalent to a gate capacitance, we obtain:

$$\frac{x \cdot C_m}{4 \cdot C_g + L \cdot C_s} = \frac{x \cdot k_v}{4 \cdot C_g/C_s + L} \leq \frac{1}{10} \quad \text{and}$$
$$x \leq \frac{4 \cdot C_g/C_s + L}{10 \cdot k_v}, \tag{7}$$

where, C_s is the capacitance from the dynamically driven wire to the substrate per unit length. We know that x can never be larger than $2 \cdot L$ (a neighbor on each side) and therefore there is a shortest length of a dynamically driven wire for which we need to apply the rule in (7). This critical length is calculated to about 160 μm for both poly, metal1 and metal2 in our process. In a similar way, we can specify design rules to avoid crosstalk due to crossing wires shown in Fig. 7(b). The unavoidable source/drain capacitances will balance the mutual capacitance if the number of crossings is limited. In our process four gate capacitances ($2C_g + C_d + C_s \approx 4C_g$) balance 6 poly-M1, 8 poly-M2 or 3 M1-M2 crossings. E.g., if a wire has less than 6 poly-M1 crossings (and no other crossings) the noise is guaranteed to be less than Vdd/10.

In this section we demonstrated methods to determine layout design rules for dynamically driven nodes, which turn out to not be very restrictive for our process. However, the design rules are strongly dependent on process parameters. For an SOI structure we can expect a much smaller capacitance from a wire to the substrate than for a bulk process. Therefore the coupling between neighboring and crossing wires will be much larger, which will put severe restrictions on layout of wires that stores charge dynamically in an SOI circuit.

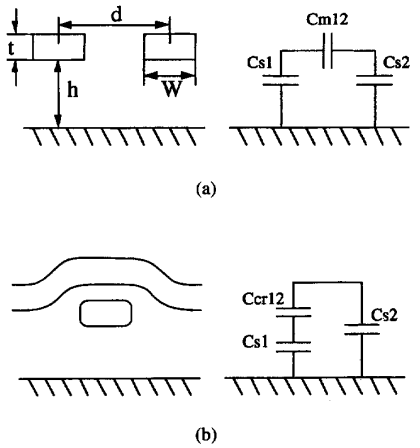


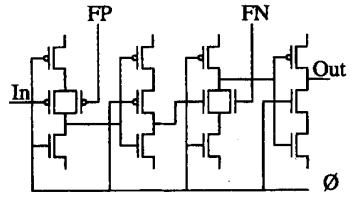
Fig. 7. (a) Geometrical and electrical model of two capacitively coupled neighboring wires. (b) Geometrical and electrical model of two capacitively coupled crossing wires.

VII. dI/dt Noise Measurement

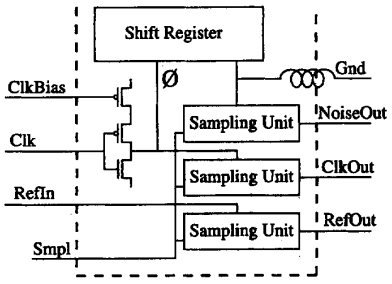
To measure noise generation of precharged dynamic logic, we designed a chip with a 96-bit shift register containing precharged N and P latches. The latches were provided with a reset signal shown in Fig. 8(a) so that both N and P blocks will generate current pulses in the ground wire at rising clock edge. Therefore (6) predicts the maximum noise amplitude when FP is low and FN is high. Since the noise amplitude depends on the clock rise time, the clock buffer was designed to have variable rise time, as in Fig. 8(b). SPICE simulations indicated a rise time varying between 0.4 ns and 1.1 ns. Clock rise times in the range of 0.4 and 1.2 ns were measured on the chip.

To measure rise times and noise pulses in the subnanosecond range with CMOS circuits, we borrow ideas from a sampling oscilloscope. If the measured signal is periodic, we can take a single sample in each period and still recover the signal shape [13], [14]. If the first sample is taken at time 0 in the first period and consecutive samples are taken at $k \cdot (T + \Delta t)$, where T is the period of the measured signal, the time resolution will be Δt. The off chip speed requirement is determined by T, which shows that low speed CMOS drivers are sufficient even though the measured signal has very high bandwidth.

The noise measurement chip was supplied with three sample units with 5 GHz input bandwidth. This extreme bandwidth was obtained by reducing the absolute accuracy. Instead we used one of the sample units as a time and voltage reference with external input. The sampled version of this reference signal was compared with the measured signals so that we could determine both amplitude and timing properties of a measured signal. One sampling unit was provided with the clock signal to measure the rise time of the clock edge. Another sampling unit measured the noise glitch on the ground level of the shift register. The whole chip, illustrated in Fig. 8(b), contains a 96-bit shift register, a clock buffer and the three sampling units.



(a)



(b)

Fig. 8. (a) A bit cell of the noise generating shift register. (b) Block schematic of the noise measurement chip. The dashed line represents the chip edges.

When making the chip layout, the effect of leakage current through the substrate could not be avoided. The model we wanted to obtain is shown in Fig. 5(b) but the substrate contacts and the relatively low resistance substrate make the model appear as in Fig. 9. The noise generating shift register is represented with the 96 PN blocks to the left. To reduce noise generation of the clock driver and induced noise in the analog part, on-chip decoupling capacitance was included. Both the clock driver and the analog circuits were supplied with separate Vdd and Gnd. The resistances drawn in Fig. 9, estimated to 1 kω each, make the model differ significantly from Fig. 5(b). The result of a spice simulation of a ground glitch caused by the shift register at a clock rise time of 0.4 ns is shown in Fig. 10(a). The voltage scale for the ground level has been magnified by a factor of two as indicated. Fig. 10(b) shows a photo from an oscilloscope when measuring the clock rise time and the ground glitch. The bottom trace shows the ground glitch with a 0.5 V scale. The middle trace is the rising clock with a rise time of 0.4 ns and a scale of 1 V per division. The top trace is an external input with a 3 V step. The overshoot reaches about 3.5 V externally before it is cut off by the sampling unit. The input stage of the sampling unit consists of an N type pass transistor [14], which makes it impossible to sample any higher value. This is also valid for the clock signal and we estimated clock rise times by linear extrapolation of the sampled rising edge. Measurement results from the chip and simulation data of the model in Fig. 9 are presented in Table II. Very accurate timing measurement was obtained using the sampling unit with an external input. A

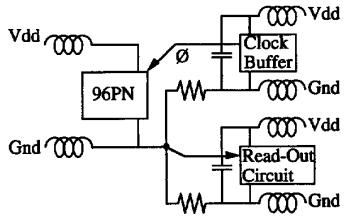
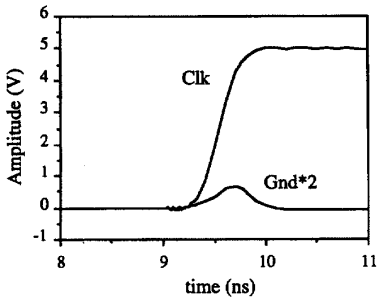
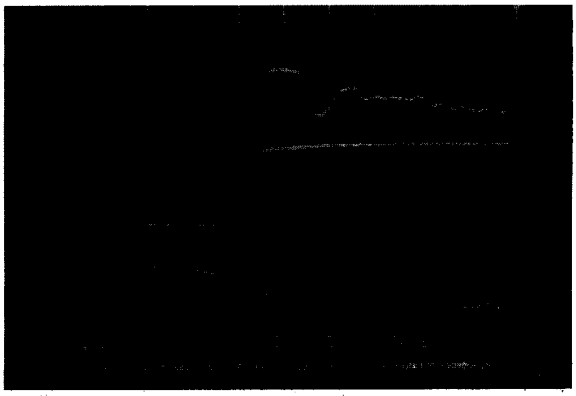


Fig. 9. Circuit model of the noise generating chip.



(a)



(b)

Fig. 10. (a) SPICE output of a 0.3 V Gnd glitch at a clock rise time of 0.4 ns. Voltage scale for Gnd is different from the clock as indicated. (b) Photo of an oscilloscope screen showing a reference input, the rising clock signal and a ground glitch generated by the shift register.

signal generator with 0.1 ns delay resolution made it possible to change the skew between the external input signal and the clock signal. By positioning the input signal at the start of the clock edge and then slightly increase the skew, we could determine clock rise times with 0.1 ns resolution. With the same measurement method, the noise pulse width was determined to be about 1 ns agreeing well with simulation data.

VIII. Decoupling Capacitance

A well known technique to reduce dI/dt noise is to provide decoupling capacitance close to chips on a PC

TABLE II
SIMULATED AND MEASURED DATA FROM THE NOISE GENERATING CHIP

Vdd	Clock Rise Time	Measured Noise Amplitude	Simulated Noise Amplitude
5 V	1.0 ns	0.23 V	0.24 V
5 V	0.75 ns	0.25 V	0.25 V
5 V	0.4 ns	0.31 V	0.35 V
4 V	0.8 ns	0.18 V	0.17 V
4 V	0.5 ns	0.22 V	0.24 V

board. Lately, decoupling capacitance has also been provided on-chip [5] to reduce the effect of the inductance in the power supply path. With continuous scaling of the minimum feature size and increasing number of transistors on a chip, the noise generated by circuits on chip will increase. This implies that on-chip decoupling capacitance will be required in the future unless new packaging techniques can drastically reduce the power supply inductance.

Including on-chip decoupling capacitance in Fig. 5(b) will make any detailed mathematical analysis difficult. However, it is possible to estimate an upper limit for the noise amplitude if the circuit is seen as disconnected from the bonding wire as in Fig. 11(a) where $i_d = i_{\text{gnd}}$. After the rising edge of $\emptyset$, charge redistribution will cause the power supply to drop ΔV and the ground level to rise ΔV, where,

$$\Delta V = \frac{\text{Vdd} \cdot C_s}{2(C_d + C_s)}. \tag{8}$$

C_s is the effective switched capacitance and C_d is the on-chip decoupling capacitance. The maximum noise amplitude of the 96-bit shift register provided with different amount of on-chip capacitance is shown in Fig. 11(b). Ground is supplied by a bonding wire with 10 nH inductance. (8) is also plotted, which shows that this formula is quite accurate for large values of C_d/C_s.

An important issue when supplying a circuit with on-chip decoupling capacitance is how to determine C_s. The effective switched capacitance of the shift register cell in Fig. 8(a) consists of two parts, capacitance related to P transistors (pcap) and to N transistors (ncap). With the same reasoning as deriving (2) from Fig. 5(b), we realize that pcap is the sum of all capacitance of falling nodes (gate, drain or source) of P transistors and ncap is the sum of all capacitance of rising nodes of N transistors. The effective switched capacitance for a bit cell of the shift register was estimated to 76.2 fF in our process including the last stage clock buffer. This agrees well with an estimate by a SPICE simulation, which indicated an effective switched capacitance of 80 fF. Keeping the power supply fluctuations below Vdd/10 requires $C_d = 4 \cdot C_s = 4 \cdot 80 \cdot 96 = 31$ pF of decoupling capacitance. A dense hand-made full-custom layout of the 96-bit shift register occupied an area of 200 × 840 μm and if the gate-to-channel capacitance of a transistor is used as the decoupling capacitance, it would add 25% area unless it is placed below Vdd and Gnd wiring or data buses as in [5]. If we assume that the probability for a bit cell containing 1 or 0 is equally likely, every second latch will not generate any current pulse. Therefore, the same decoupling capacitance would be enough to supply a twice as large shift register.

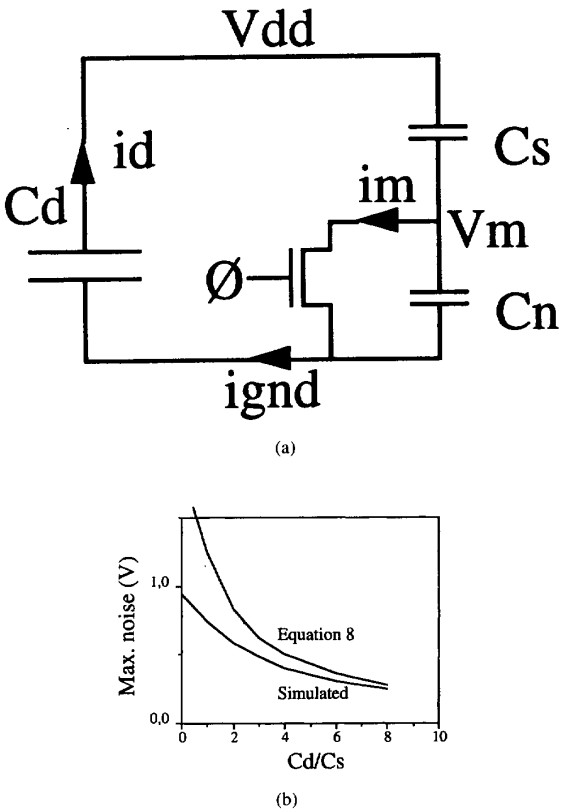


Fig. 11. (a) Worst case analysis of the effect of decoupling capacitance (Cd) is obtained when power supplying bonding wires are seen as being cutoff. (b) Maximum noise amplitude for the 96-bit shift register with on-chip decoupling capacitance.

IX. CONCLUSION

In this paper we discuss noise in dynamic logic. Our major conclusion is that it is possible to design large scale systems utilizing the advantages of dynamic logic but we need to obey some process-dependent design rules that are more strict for dynamic logic than for static logic. For example, we need lots of on-chip decoupling capacitance to reduce dI/dt noise and there are restrictions on the physical layout of dynamically driven wires to avoid crosstalk.

The noise sensitivity of dynamic logic is larger than that of static logic. However, it is possible to improve the noise margin of dynamic logic significantly, utilizing weak feedback. The effect of a noise pulse depends on both the amplitude and the width of the pulse. A more narrow pulse can have larger amplitude without causing logical errors. This has been observed for static logic but here we show the same phenomena in dynamic circuits. A main difference between static and dynamic logic is that the output of a dynamic latch might get stuck at the peak value of a narrow glitch so that the following circuit receives an

extended noise pulse during half a clock period. With this observation we concluded that the folklore rule saying "a dynamic node should not drive another dynamic node" is important for large scale systems.

Static and dynamic flip-flops generate about the same noise levels internally. It is easy to believe that precharged logic will generate more noise than static, but this is not the case as shown here. Therefore, internally generated noise is mainly dependent on the number of latches and D elements determined by the degree of pipelining. This is true for small logic depths discussed in this paper. For domino chains, each precharged node will generate a current pulse equivalent to the current in a precharged latch. This has to be taken into account when estimating noise levels and required on-chip decoupling capacitance.

Two chips were designed, one for measuring the noise margin of different latches and another chip to measure the noise generation of precharged latches. The noise margin of V_t and the method to increase the noise margin using weak feedback was verified. The measurements of noise generation verified that the simulation model used gave a good description of the real power supply noise amplitude.

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